1.6 V, Micropower 12-Bit ADC

Known Good Die

AD7466-KGD

FEATURES

- **Specified for V_{DD} of 1.6 V to 3.6 V**
- **Low power**
  - **0.62 mW typical at 100 kSPS with 3 V supplies**
  - **0.48 mW typical at 50 kSPS with 3.6 V supplies**
  - **0.12 mW typical at 100 kSPS with 1.6 V supplies**
- **Fast throughput rate: 200 kSPS**
- **Wide input bandwidth: 71 dB SNR at 30 kHz input frequency**
- **Flexible power/serial clock speed management**
- **No pipeline delays**
- **High speed serial interface**
  - **SPI/QSPI™/MICROWIRE™/DSP compatible**
- **Automatic power-down**
- **Power-down mode: 8 nA typical**

FUNCTIONAL BLOCK DIAGRAM

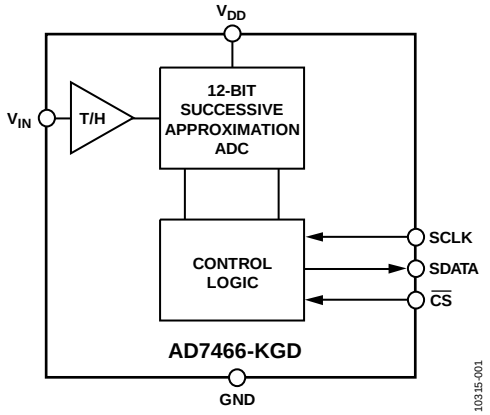

Figure 1.

APPLICATIONS

- **Battery-powered systems**
- **Medical instruments**
- **Remote data acquisition**
- **Isolated data acquisition**

GENERAL DESCRIPTION

The AD7466-KGD[1] are 12-bit, high speed, low power, successive approximation analog-to-digital converter (ADC). The part operates from a single 1.6 V to 3.6 V power supply and features throughput rates up to 200 kSPS with low power dissipation. The part contains a low noise, wide bandwidth track-and-hold amplifier, which can handle input frequencies in excess of 3 MHz.

The conversion process and data acquisition are controlled using $\overline{CS}$ and the serial clock, allowing the device to interface with microprocessors or DSPs. The input signal is sampled on the falling edge of $\overline{CS}$, and the conversion is also initiated at this point. There are no pipeline delays associated with the part.

The reference for the part is taken internally from V_{DD}. This allows the widest dynamic input range to the ADC. Thus, the analog input range for the part is 0 V to V_{DD}. The conversion rate is determined by the SCLK.

[1] Protected by U.S. Patent No. 6,681,332.

PRODUCT HIGHLIGHTS

1. Specified for supply voltages of 1.6 V to 3.6 V.
2. High throughput rate with low power consumption. Power consumption in normal mode of operation at 100 kSPS and 3 V is 0.9 mW maximum.
3. Flexible power/serial clock speed management. The conversion rate is determined by the serial clock, allowing the conversion time to be reduced through increases in the serial clock speed. Automatic power-down after conversion allows the average power consumption to be reduced when in power-down. Current consumption is 0.1 μA maximum and 8 nA typically when in power-down.
4. Reference derived from the power supply.
5. No pipeline delay.
6. The part features a standard successive approximation ADC with accurate control of conversions via a $\overline{CS}$ input.

Rev. 0

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REVISION HISTORY

11/11—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 1.6 V to 3.6 V, f_{SCLK} = 3.4 MHz, f_{SAMPLE} = 100 kSPS, unless otherwise noted. $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. The temperature range for the AD7466-KGD version is −40°C to +85°C.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE					f_{IN} = 30 kHz sine wave
Signal-to-Noise and Distortion (SINAD)	69			dB	1.8 V ≤ V_{DD} ≤ 2 V
	70			dB	2.5 V ≤ V_{DD} ≤ 3.6 V
		70		dB	V_{DD} = 1.6 V
Signal-to-Noise Ratio (SNR)	70			dB	1.8 V ≤ V_{DD} ≤ 2 V
		71		dB	1.8 V ≤ V_{DD} ≤ 2 V
	71			dB	2.5 V ≤ V_{DD} ≤ 3.6 V
		70.5		dB	V_{DD} = 1.6 V
Total Harmonic Distortion (THD)		−83		dB	
Peak Harmonic or Spurious Noise (SFDR)		−85		dB	
Intermodulation Distortion (IMD)					fa = 29.1 kHz, fb = 29.9 kHz
Second-Order Terms		−84		dB	
Third-Order Terms		−86		dB	
Aperture Delay		10		ns	
Aperture Jitter		40		ps	
Full Power Bandwidth		3.2		MHz	At 3 dB, 2.5 V ≤ V_{DD} ≤ 3.6 V
		1.9		MHz	At 3 dB, 1.6 V ≤ V_{DD} ≤ 2.2 V
		750		kHz	At 0.1 dB, 2.5 V ≤ V_{DD} ≤ 3.6 V
		450		kHz	At 0.1 dB, 1.6 V ≤ V_{DD} ≤ 2.2 V
DC ACCURACY					Maximum specifications apply as typical figures when V_{DD} = 1.6 V
Resolution		12		Bits	
Integral Nonlinearity			±1.5	LSB	
Differential Nonlinearity			−0.9/+1.5	LSB	Guaranteed no missed codes to 12 bits
Offset Error			±1	LSB	
Gain Error			±1	LSB	
Total Unadjusted Error (TUE)			±2	LSB	
ANALOG INPUT					
Input Voltage Range	0		V_{DD}	V	
DC Leakage Current			±1	µA	
Input Capacitance		20		pF	
LOGIC INPUTS					
Input High Voltage, V_{INH}	0.7 × V_{DD}			V	1.6 V ≤ V_{DD} < 2.7 V
	2			V	2.7 V ≤ V_{DD} ≤ 3.6 V
Input Low Voltage, V_{INL}			0.2 × V_{DD}	V	1.6 V ≤ V_{DD} < 1.8 V
			0.3 × V_{DD}	V	1.8 V ≤ V_{DD} < 2.7 V
			0.8	V	2.7 V ≤ V_{DD} ≤ 3.6 V
Input Current, I_{IN}, SCLK Pin			±1	µA	Typically 20 nA, V_{IN} = 0 V or V_{DD}
Input Current, I_{IN}, $\overline{CS}$ Pin		±1		µA	
Input Capacitance, C_{IN}			10	pF	Sample tested at 25°C to ensure compliance
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	V_{DD} − 0.2			V	I_{SOURCE} = 200 µA, V_{DD} = 1.6 V to 3.6 V
Output Low Voltage, V_{OL}			0.2	V	I_{SINK} = 200 µA
Floating-State Leakage Current			±1	µA	
Floating-State Output Capacitance			10	pF	
Output Coding	Straight (natural) binary				

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CONVERSION RATE					
Conversion Time			4.70	µs	16 SCLK cycles with SCLK at 3.4 MHz
Throughput Rate			200	kSPS	
POWER REQUIREMENTS					
V_{DD}	1.6		3.6	V	
I_{DD}					Digital inputs = 0 V or V_{DD}
Normal Mode (Operational)			300	µA	V_{DD} = 3 V, f_{SAMPLE} = 100 kSPS
		110		µA	V_{DD} = 3 V, f_{SAMPLE} = 50 kSPS
		20		µA	V_{DD} = 3 V, f_{SAMPLE} = 10 kSPS
			240	µA	V_{DD} = 2.5 V, f_{SAMPLE} = 100 kSPS
		80		µA	V_{DD} = 2.5 V, f_{SAMPLE} = 50 kSPS
		16		µA	V_{DD} = 2.5 V, f_{SAMPLE} = 10 kSPS
			165	µA	V_{DD} = 1.8 V, f_{SAMPLE} = 100 kSPS
		50		µA	V_{DD} = 1.8 V, f_{SAMPLE} = 50 kSPS
		10		µA	V_{DD} = 1.8 V, f_{SAMPLE} = 10 kSPS
Power-Down Mode			0.1	µA	SCLK on or off, typically 8 nA
Power Dissipation					
Normal Mode (Operational)			0.9	mW	V_{DD} = 3 V, f_{SAMPLE} = 100 kSPS
			0.6	mW	V_{DD} = 2.5 V, f_{SAMPLE} = 100 kSPS
			0.3	mW	V_{DD} = 1.8 V, f_{SAMPLE} = 100 kSPS
Power-Down Mode			0.3	µW	V_{DD} = 3 V

TIMING SPECIFICATIONS

For all devices, V_{DD} = 1.6 V to 3.6 V; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Sample tested at 25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.4 V.

Table 2.

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Description
f_{SCLK}	3.4	MHz max	Mark/space ratio for the SCLK input is 40/60 to 60/40.
	10	kHz min	1.6 V ≤ V_{DD} ≤ 3 V; minimum f_{SCLK} at which specifications are guaranteed.
	20	kHz min	V_{DD} = 3.3 V; minimum f_{SCLK} at which specifications are guaranteed.
	150	kHz min	V_{DD} = 3.6 V; minimum f_{SCLK} at which specifications are guaranteed.
$t_{CONVERT}$	16 × t_{SCLK}		
Acquisition Time			Acquisition time/power-up time from power-down. The acquisition time is the time required for the part to acquire a full-scale step input value within ±1 LSB or a 30 kHz ac input value within ±0.5 LSB.
	780	ns max	V_{DD} = 1.6 V.
	640	ns max	1.8 V ≤ V_{DD} ≤ 3.6 V.
t_{QUIET}	10	ns min	Minimum quiet time required between bus relinquish and the start of the next conversion.
t_1	10	ns min	Minimum $\overline{CS}$ pulse width.
t_2	55	ns min	$\overline{CS}$ to SCLK setup time. If V_{DD} = 1.6 V and f_{SCLK} = 3.4 MHz, t_2 has to be 192 ns minimum in order to meet the maximum figure for the acquisition time.
t_3	55	ns max	Delay from $\overline{CS}$ until SDATA is three-state disabled. Measured with the load circuit in Figure 2 and defined as the time required for the output to cross the V_{IH} or V_{IL} voltage.
t_4	140	ns max	Data access time after SCLK falling edge. Measured with the load circuit in Figure 2 and defined as the time required for the output to cross the V_{IH} or V_{IL} voltage.
t_5	0.4 t_{SCLK}	ns min	SCLK low pulse width.
t_6	0.4 t_{SCLK}	ns min	SCLK high pulse width.
t_7	10	ns min	SCLK to data valid hold time. Measured with the load circuit in Figure 2 and defined as the time required for the output to cross the V_{IH} or V_{IL} voltage.
t_8	60	ns max	SCLK falling edge to SDATA three-state. t_8 is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit in Figure 2. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_8, quoted in the timing characteristics, is the true bus relinquish time of the part, and is independent of the bus loading.
	7	ns min	SCLK falling edge to SDATA three-state.

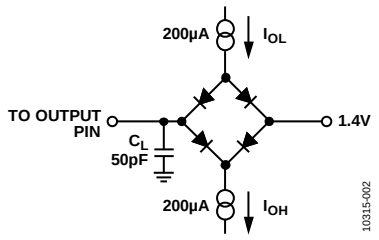

Figure 2. Load Circuit for Digital Output Timing Specifications

TIMING EXAMPLES

Figure 3 shows some of the timing parameters from Table 2 in the Timing Specifications section.

Timing Example 1

As shown in Figure 3, f_{SCLK} = 3.4 MHz and a throughput of 100 kSPS gives a cycle time of $t_{CONVERT} + t_8 + t_{QUIET}$ = 10 µs. Assuming V_{DD} = 1.8 V, $t_{CONVERT} = t_2 + 15(1/f_{SCLK})$ = 55 ns + 4.41 µs = 4.46 µs, and t_8 = 60 ns maximum, then t_{QUIET} = 5.48 µs, which satisfies the requirement of 10 ns for t_{QUIET}. The part is fully powered up and the signal is fully acquired at Point A. This means that the acquisition/power-up time is $t_2 + 2(1/f_{SCLK})$ = 55 ns + 588 ns = 643 ns, satisfying the maximum requirement of 640 ns for the power-up time.

Timing Example 2

The AD7466-KGD can also operate with slower clock frequencies. As shown in Figure 3, assuming V_{DD} = 1.8 V, f_{SCLK} = 2 MHz, and a throughput of 50 kSPS gives a cycle time of $t_{CONVERT} + t_8 + t_{QUIET}$ = 20 µs. With $t_{CONVERT} = t_2 + 15(1/f_{SCLK})$ = 55 ns + 7.5 µs = 7.55 µs, and t_8 = 60 ns maximum, this leaves t_{QUIET} to be 12.39 µs, which satisfies the requirement of 10 ns for t_{QUIET}. The part is fully powered up and the signal is fully acquired at Point A, which means the acquisition/power-up time is $t_2 + 2(1/f_{SCLK})$ = 55 ns + 1 µs = 1.05 µs, satisfying the maximum requirement of 640 ns for the power-up time. In this example and with other slower clock values, the part is fully powered up and the signal already acquired before the third SCLK falling edge; however, the track-and-hold does not go into hold mode until that point. In this example, the part can be powered up and the signal can be fully acquired at approximately Point B in Figure 3.

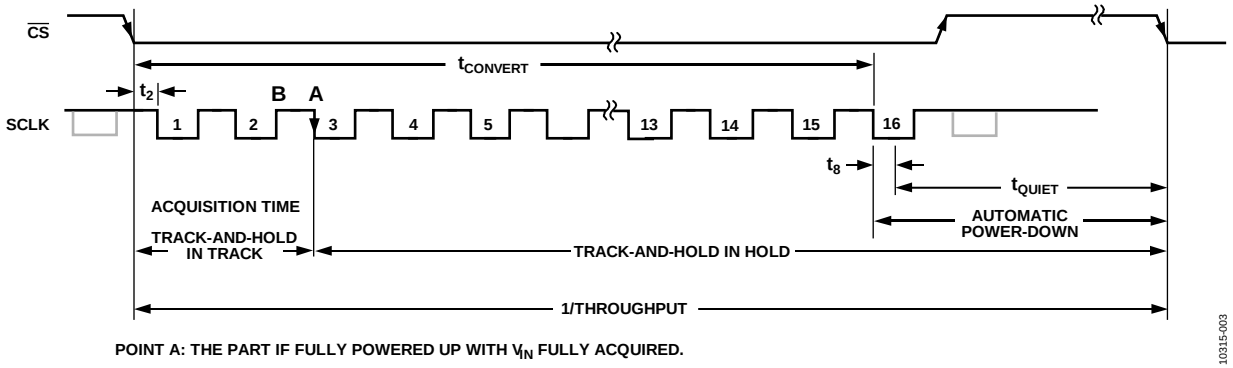

Figure 3. AD7466-KGD Serial Interface Timing Diagram Example

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted. Transient currents of up to 100 mA do not cause SCR latch-up.

Table 3.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
Analog Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to GND	−0.3 V to +7 V
Digital Output Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Input Current to any Pin Except Supplies	±10 mA
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
ESD	3.5 kV

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PAD CONFIGURATION AND FUNCTION DESCRIPTIONS

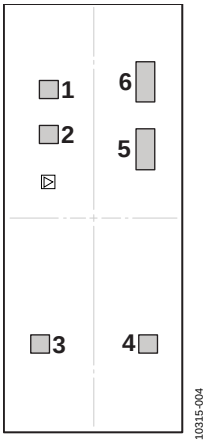

Figure 4. Pad Configuration

Table 4. Pad Function Descriptions

Pad No.	X-Axis (µm)	Y-Axis (µm)	Mnemonic	Pad Type	Description
1	−173	+634	$\overline{CS}$	Single	Chip Select. Active low logic input. This input provides the dual function of initiating conversions on the devices and frames the serial data transfer.
2	−173	+494	SDATA	Single	Data Out. Logic output. The conversion result from the AD7466-KGD is provided on this output as a serial data stream. The bits are clocked out on the falling edge of the SCLK input. The data stream from the AD7466-KGD consists of four leading zeros followed by the 12 bits of conversion data, provided MSB first.
3	−187	−600	SCLK	Single	Serial Clock. Logic input. SCLK provides the serial clock for accessing data from the parts. This clock input is also used as the clock source for the conversion process of the parts.
4	+187	−600	V_{IN}	Single	Analog Input. Single-ended analog input channel. The input range is 0 V to V_{DD}.
5A	+173	+447.6	GND	Double	Analog Ground. Ground reference point for all circuitry on the devices. All analog input signals should be referred to this GND voltage.
5B	+173	+489.6	GND	Double	Analog Ground. Ground reference point for all circuitry on the devices. All analog input signals should be referred to this GND voltage.
6A	+173	+637.6	V_{DD}	Double	Power Supply Input. The V_{DD} range for the devices is from 1.6 V to 3.6 V.
6B	+173	+679.6	V_{DD}	Double	Power Supply Input. The V_{DD} range for the devices is from 1.6 V to 3.6 V.

OUTLINE DIMENSIONS

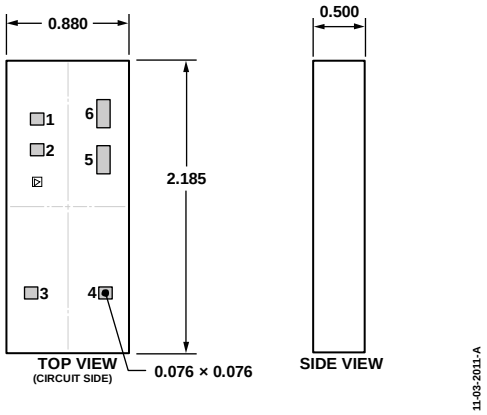

Figure 5. 6-Pad Bare Die [CHIP]
(C-6-4)
Dimensions shown in millimeters

DIE SPECIFICATIONS AND ASSEMBLY RECOMMENDATIONS

Table 5. Die Specifications

Parameter	Value	Unit
Chip Size	660 (x) × 2015 (y)	µm
Scribe Line Width	120 (x) × 170 (y)	µm
Die Size	880 (x) × 2185 (y)	µm
Thickness	500	µm
Backside	Silicon	Not applicable
Passivation	Nitride	Not applicable
Bond Pads (Minimum Size)	76 × 76	µm
Bond Pad Composition	98.5% Al, 1% Si, 0.5% Cu	%
ESD	3.5	kV

Table 6. Assembly Recommendations

Assembly Component	Recommendation
Die Attach	Epoxy adhesive
Bonding Method	Gold ball or aluminum wedge
Bonding Sequence	Five First

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD7466-KGD-DF	−40°C to +85°C	6-Pad Bare Die [CHIP]	C-6-4

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